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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,803	11/04/2003	Masahiro Yoshida	1248-0677P	4032

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,803	YOSHIDA, MASAHIRO	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 4 August 2006. Claims 1-20 are pending.

Response to Arguments

2. Applicant's arguments filed the 4 August 2006 have been fully considered but they are not persuasive.

On page 9, 5th paragraph of the applicant's response the applicant argues the rejection of claims 1, 2, 4, 6, 7, 9, 11, 12 , 14 and 16 as rejected under 35 U.S.C. § 102(a) as being anticipated by AAPA. In the applicant's argument the applicant accuses the examiner of misunderstanding the description of the AAPA. The applicant further argues that the lines to which the examiner refers to do not mean that a capacitance is formed intentionally by that the capacitance is naturally generated, and thus, it is "clear that AAPA does not teach or suggest a "first capacitance formed" on at least one first bus line. The examiner respectfully disagrees.

First, the examiner does understand the difference between the applicant's invention and the AAPA. Essentially the applicant's invention involves adding a capacitor to the lines on the main display that are not connected to the lines on the smaller second display such that the capacitance on all of the display lines, regardless of being connected to the second display or not, will be equal. However, this is **not**

what is claimed. The claims only recite that "at least one of the first bus lines has a first capacitance formed thereon," which as explained in the rejection of claims 1, 6-7 and 12, is described on page 4, line 18 to page 5, line 5 of the applicant's specification where it states: "the source bus lines in the group 196 of Figure 25 have a capacitance of 20 pF **formed** on them." The claims **do not** recite that this formed capacitance is a result of adding a capacitor to the display lines not connected to the second display panel or even how the capacitance is formed, i.e. whether it is "intentional" or "natural." Therefore, AAPA anticipates independent claims 1, 6-7 and 12. If it is the applicant's intention to claim the difference, the claim language should be changed so that the limitation of a capacitor is added and it is clear that the capacitance that is formed by the capacitor is added to the existing capacitance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-2, 4, 6-7, 9, 11-12, 14 and 16-20 are rejected under 35 U.S.C. 102(a) as being anticipated by AAPA (Figure 25 and page 1, line 10 to page 5, line 9 of the specification.).

Regarding claims 1, 6 and 7, AAPA discloses an active matrix substrate, a display comprising an active matrix substrate and a display comprising display panels each including an active matrix substrate (Figure 25 shows a twin-panel display 181 as explained on page 1, line 12 to page 2, line 2. The main panel 182 includes a TFT substrate 184 as explained on page 2 lines 3-5 and the sub-panel 183 includes a TFT substrate 186 as explained on page 3, lines 1-2.) comprising:

first bus lines and second bus lines arranged to form a matrix (Figure 25 shows that source bus lines 189 and gate bus lines 188 are arranged to form a matrix.);

devices provided near respective intersections of the first bus lines and the second bus lines (Figure 25 shows that TFTs 192 are laid out near the intersections of the gate bus lines 188 and the source bus lines 189 as explained on page 2, lines 10-12.); and

switching pixel electrodes electrically connected to the first bus lines and the second bus lines through the switching devices (Page 2, lines 12-18 explain that the pixel electrode is connected to the first and second bus lines through TFTs 192.), wherein:

at least one of the first bus lines has a first capacitance formed thereon (Page 4, line 18 to page 5, line 1 explain that the source bus lines in the group 196 shown in Figure 25 have a capacitance of 20 pF formed on them.); and

the first bus lines, except for the at least one first bus line with a first capacitance, are connected to first bus lines on another active matrix substrate (Figure 25 shows that

the group 195 of source bus lines which does not include the first group 196 containing the 20 pF are connected to the source bus lines of the active matrix substrate 187.).

Regarding claim 2, AAPA discloses the active matrix substrate as set forth in claim 1, wherein the at least one first bus line (Figure 25, group 196) with a first capacitance (20 pF as explained in the rejection of claim 1.) is connected to a line connected to no pixel electrode on the other active matrix substrate (Figure 25 shows that the group 196 of source bus lines 189 are connected to the gate bus lines 188 which are not connected to a pixel electrode of the active matrix substrate 187.).

Regarding claim 4, AAPA discloses the active matrix substrate as set forth in claim 1, wherein the first bus lines are connected to a source driver (Figure 25 shows that the first bus lines 189 are connected to the source driver 191.), and the second bus lines are connected to a gate driver (Figure 25 shows that the second bus lines 188 are connected to the gate driver 190.).

Regarding claim 9, this claim is rejected under the same rationale as claim 4.

Regarding claim 11, AAPA discloses the display as set forth in claim 7, wherein one of the display panels is designated as a main panel (Figure 25, main panel 182), and the display panels, except for the main panel, are designated as sub-panels having less display pixels than the main panel (Figure 25, sub-panel 183).

Regarding claim 12, please refer to the rejection of claims 1, 6 and 7, and further more AAPA discloses wherein:

the first bus lines are shared for use among the display panels (Figure 25, the group 195 of first bus lines 189 are shared between the display panel 182 and display panel 183.);

in at least one of the display panels, at least one of the first bus lines is connected to none of the pixel electrodes on the active matrix substrate (Figure 25 shows that group 196 of first bus lines 189 are not connected to pixel electrodes on panel 183.); and

the at least one first bus line connected to none of the pixel electrodes has a first capacitance formed thereon (Page 4, line 18 to page 5, line 1 explain that the source bus lines in the group 196 shown in Figure 25 have a capacitance of 20 pF formed on them.).

Regarding claim 14, this claim is rejected under the same rationale as claim 4.

Regarding claim 16, this claim is rejected under the same rationale as claim 11.

Regarding claims 17-20, AAPA discloses the active matrix substrates as set forth in claims 1, 6-7 and 12, wherein an amount of the first capacitance is such that there is substantially no difference in signal delay on each first bus line of the active

matrix substrate that is connected to a first bus line on the other active matrix substrate and signal delay on the at least one first bus line with a first capacitance (The examiner interprets that since the AAPA discloses the same structure which is claimed in claims 1, 6-7 and 12 that the structure of the AAPA would do the same thing as the claimed structure, meaning that there would be *substantially* no difference in signal delay.).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 3, 5, 8, 10, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (Figure 25 and page 1, line 10 to page 5, line 9 of the specification.) in view of Kurashima et al. (US 6,954,184).

Regarding claim 3, AAPA discloses the active matrix substrate as set forth in claim 1.

AAPA also discloses that each of those first bus lines connected to the second active matrix substrate (Group 195 are a part of the first bus lines 189 connected to the sub-panel 182.) has a second capacitance formed thereon from the sub-panel 183 which is less than the first capacitance (Page 4, line 18 to page 5, line 1 explain that the group 195 has a capacitance of 10 pF formed on them from the sub-panel 183 which is less than the contributing first capacitance, 20 pF, of the main panel 182.).

AAPA fails to disclose that the group of first bus lines connected to the second active matrix substrate have no first capacitance formed thereon.

Kurashima et al. disclose a drive IC for driving different displays which can be shared where no scanning signal is supplied to the main display 1A shown in Figure 5 when a scanning signal is sent to the sub-display 2A as explained in column 10, lines 34-40.

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the method of only supplying scanning signals to the sub-display when the sub-display data is being written as taught by Kurashima et al. with the active matrix substrate taught by AAPA such that the capacitance of 20 pF caused by the main panel would not be caused to effect the sub-panel meaning that the second group pf lines would contain 10 PF which is less than the first capacitance of 20

pF, in order to reduce the power consumed by the display when the panels are concurrently driven.

Regarding claim 5, AAPA discloses the active matrix substrate as set forth in claim 1.

AAPA fails to teach wherein the first bus lines are connected to a gate driver, and the second bus lines are connected to a source driver.

Kurashima et al. discloses that although wires are shared to which a scanning signal is supplied (Figure 13 and column 20, lines 22-28.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the first bus lines as taught by AAPA to be the ones connected to the gate driver as taught by Kurashima et al. such that the scanning liens would be the lines shared among the two display panels in order to allow for an alternative arrangement to be used for the placement of the sub-panel.

Regarding claim 8, this claim is rejected under the same rationale as claim 3.

Regarding claim 10, this claim is rejected under the same rationale as claim 5.

Regarding claim 13, this claim is rejected under the same rationale as claim 3.

Regarding claim 15, this claim is rejected under the same rationale as claim 5.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

22 August 2006

AMR A. AWAD
PRIMARY EXAMINER